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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,166	01/18/2002	Hiroshi Horibe	50090-466	7602

7590 12/17/2003

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/050,166	HORIBE, HIROSHI	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- Th MAILING DATE of this communication appears n the cov r sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 12-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

The claim limitations as recited in the claim 1, line 10 and claim 2, line 2 include: "conductive parts on said chip".

Therefore, the conductive parts on said chip must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Proposed amendments/corrections to Figure 7A indicating the conductive parts, as specified in the Remarks (paper # 10), have not been received in any attachments/photocopy in the paper #10.

Information Disclosure Statem nt

3. The Information Disclosure Statement filed on 01-18-02 has been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Shigeno et al. (US Pat. 6372625).

Regarding claim 4, Shigeno et al. disclose a semiconductor device comprising:

- a chip (11 in Fig. 2) provided with an insulating/passivating layer/part (not numerically referenced in Fig. 2; Col. 3, line 52) and a plurality of bonding pads (12 in Fig. 2)
- a plurality of inner leads (15 in Fig. 2) arranged opposite/at a distance from the bonding pads
- a plurality of bonding wires (16 in Fig. 2) electrically connecting the boding pads and the corresponding inner leads

- each of the bonding wires having a plurality of bends, the bends having a range of bending angles (23, 24, 25, etc. in Fig. 2; Col. 4, lines 40-50), being electrically isolated from other conductive pads/parts on the chip and being arranged at an optional/desired positions on a surface of the chip, and
- the bonding wires and the inner leads being sealed in a resin (17 in Fig. 2) package such that one of the bends (see 23 in dotted line configuration in Fig. 2) is exposed on the surface of the resin package (Col. 4, line 62)

(Fig. 2 and 5; Col. 3, line 40- Col. 5, line 60).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

7. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeno et al. (US Pat. 6372625) in view of Kumazawa et al. (US Pat. 5156323).

Regarding claim 1, Shigeno et al. disclose a semiconductor device comprising:

- a chip (11 in Fig. 2) provided with an insulating/passivating layer/part (not numerically referenced in Fig. 2; Col. 3, line 52) and a plurality of exposed bonding pads (12 in Fig. 2)
- a plurality of inner leads (15 in Fig. 2) arranged opposite/at a distance from the bonding pads
- a plurality of bonding wires (16 in Fig. 2) electrically connecting the boding pads and the corresponding inner leads
- each of the bonding wires having a plurality of bends, the bends having a range of bending angles (23, 24, 25, etc. in Fig. 2; Col. 4, lines 40-50), the bends being electrically isolated from other conductive pads/parts on the chip and being arranged at an optional/desired positions on a surface of the chip, and
- the bonding wires being sealed in a resin (17 in Fig. 2) package providing the isolation/insulation for the bends from the conductive parts/pads of the chip

(Fig. 2 and 5; Col. 3, line 40- Col. 5, line 60).

Shigeno et al. fail to teach the bend nearest to the inner lead being at a level higher than that nearest to the chip.

Kumazawa et al. teach using bonding wires having a plurality of bends such that the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) is at a higher level than the bend (1a in Fig. 4) nearest to bonding point on chip (A on

chip 3 in Fig. 4) to provide a protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bend nearest to the inner lead being at a level higher than that nearest to the chip as taught by Kumazawa et al. so that the edge shorting can be prevented and the length of the wire loop can be increased in Shigeno et al's device.

Regarding claim 2, Shigeno et al. and Kumazawa et al. teach substantially the entire claimed structure as applied to claim 1, wherein Shigeno et al. teach the respective bends being apart from the chip and being electrically insulated from the other conductive pads/parts of the chip.

Regarding claim 5, Shigeno et al. and Kumazawa et al. teach substantially the entire claimed structure as applied to claim 1, wherein Shigeno et al. further teach the nearest bend to the inner lead (24 in Fig. 2) being located at a position outside a range/dimensions extending over the chip, the range/dimensions being defined by the edges of the chip (see position of 24 with respect to 26 in Fig. 2).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeno et al. (US Pat. 6372625) and Kumazawa et al. (US Pat. 5156323) as applied to claim 1 above, and further in view of Wark et al. (US Pat. 5847445).

Regarding claim 3, Shigeno et al. and Kumazawa et al. teach substantially the entire claimed structure as applied to claim 1 above, except at least one of the plurality of bends being in contact with the electrically insulating part so as to be insulated from the conductive parts of the chip.

Wark et al. teach using a device with a plurality of plurality of bonding wires having bends (62 in Fig. 3 and 4) where the bends (not numerically referenced in Fig. 3 and 4- see the bend at location 72 on the insulating part 70B and 70D respectively) are in contact with electrically insulating parts (70B and 70D in Fig. 3 and 4 respectively) so as to be insulated from the conductive parts/pads of the chip, to provide support and to minimize sagging for the bonding wires (Col. 5, line 40- Col. 6, line 63).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate at least one of the plurality of bends being in contact with the electrically insulating part so as to be insulated from the conductive parts of the chip as taught by Wark et al. so that bonding wire support can be improved and the wire sagging can be reduced in Kumazawa et al. and Shigeno et al's device.

Response to Arguments

9. Applicant's arguments filed on 10-01-03 have been fully considered but they are not persuasive.

A. Applicant contends that Kumazawa et al. do not teach in Fig. 3, the bend nearest to a bonding point on a work piece/lead frame substrate not being at a higher level than the bend nearest to bonding point on chip.

However, as explained above, Kumazawa et al. teach in Fig. 4, the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) being at a higher level than the bend (1a in Fig. 4) nearest to bonding point on chip (A on chip 3 in Fig. 4) to provide protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

B. Applicant contends that the Drawing/Figure 2 in Shigeno et al. is not to scale and therefore should not be used to show the exposed bend.

However, as explained above, the bend (see 23 in dotted line configuration in Fig. 2; Col. 4, lines 62-65) of the conventional bonding wire being clearly shown as being extended and being exposed on the surface of the resin package without considering relative proportions of the bonding wire (length, diameter, etc.), the chip (length, thickness, etc.) and that of the angle of the bend measured from the Figure.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-305-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP
12-10-03

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800